

# Laxmidhar Barik

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## Carrer Objective

As a recent graduate with a keen interest in VLSI design and digital electronics, I am eager to begin my career in a dynamic and innovative company. I am excited to apply the knowledge and skills I have gained through my education to contribute effectively to hardware design and verification projects. I am committed to continuous learning and working collaboratively in a cross-functional team to make valuable contributions to the semiconductor engineering. .

## Education

| Course   | Institution              | Year      | CGPA/% |
|--|--------------------------|-----------|--------|
| Master of Technology in VLSI Design & Embedded Systems | NIT Raipur, Chhattisgarh | 2023–2025 | 9.12   |
| Bachelor of Technology in Electrical & Electronics     | BPUT, Odisha             | 2018–2022 | 9.04   |
| Intermediate (12 <sup>th</sup> )                       | CHSE, Odisha             | 2015–2017 | 83.89% |
| 10 <sup>th</sup>                                       | BSEO, Odisha             | 2015      | 88.83% |

## Certifications Workshops

- Participated in the INUP-i2i 18<sup>th</sup> User Awareness Workshop on Device Fabrication and Characterization Facility for Nanotechnology at IIT Delhi, held on 12–13 December 2024.
- Completed **Digital Electronics** online course from NPTEL.
- Completed **SystemVerilog for Verification** course from Udemy.

## Achievements

- **GATE 2023 (EE):** Qualified with an **AIR 3193**
- **GATE 2024 (EE):** Qualified with an **AIR 6005**

## Projects

1. **Vending Machine Design Using Xilinx ISE Design Suite**  
Designed a vending machine using **Verilog HDL**. Implemented the design based on the concept of a **Finite State Machine (FSM)**.
2. **FIFO and LIFO RTL Design**  
Designed a synchronous **FIFO** using **Verilog HDL**. **Xilinx ISE Design Suite** was used to implement and simulate the design.
3. **Finite State Machine Design**  
Designed a **sequence detector** using both **Moore and Mealy FSM** models. Implemented using **Verilog HDL**.
4. **Positive Edge Detector**  
Designed a **Positive Edge Detector** circuit using **Verilog HDL**.

## 5. PLL (Phase-Locked Loop) Design

March 2024 – till date

Implemented a PLL using both LTspice and Cadence Virtuoso. Designed key PLL components:

- Phase Detector
- Charge Pump Loop Filter
- Voltage-Controlled Oscillator (VCO)
- Loop Filter

## 6. Operational Transconductance Amplifier (OTA)

Designed an Operational Transconductance Amplifier (OTA) using LTspice and Cadence Virtuoso. Key tasks:

- Implemented Miller OTA
- Performed AC analysis of Miller OTA
- Simulated test circuits to measure:
  - (a) Input Offset Voltage
  - (b) Input Common Mode Voltage Range
  - (c) Maximum Output Voltage Swing
  - (d) Open-Loop Gain, Bandwidth (BW), and Gain-Bandwidth Product (GBW)
  - (e) Phase Margin and Gain Margin

# Hardware Verification Projects

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## SystemVerilog-based Testbenches

- D Flip-Flop Testbench** [github.com/Blaxmidhar/verilog-and-systemverilog/d-flipflop-sv](https://github.com/Blaxmidhar/verilog-and-systemverilog/d-flipflop-sv)  
*Developed a layered SystemVerilog testbench using class-based verification components including generator, driver, monitor, and scoreboard. Verified functionality of a D Flip-Flop with randomized input sequences and a self-checking scoreboard mechanism.*
- T Flip-Flop Testbench** [github.com/Blaxmidhar/verilog-and-systemverilog/t-flipflop-sv](https://github.com/Blaxmidhar/verilog-and-systemverilog/t-flipflop-sv)  
*Built a reusable testbench for verifying a T Flip-Flop using random stimulus generation, interface-based DUT connection, and scoreboard-driven result validation.*
- Full Adder Testbench** [github.com/Blaxmidhar/verilog-and-systemverilog/full-adder-sv](https://github.com/Blaxmidhar/verilog-and-systemverilog/full-adder-sv)  
*Created a modular SystemVerilog testbench for a Full Adder with transaction-level inputs, monitored outputs, and functional result comparison for all binary combinations.*
- 8:1 Multiplexer Testbench** [github.com/Blaxmidhar/verilog-and-systemverilog/8x1-mux-sv](https://github.com/Blaxmidhar/verilog-and-systemverilog/8x1-mux-sv)  
*Implemented stimulus-driven testbench to verify selection and data-routing logic in an 8:1 multiplexer using assertions and waveform analysis.*
- 1:8 Demultiplexer Testbench** [github.com/Blaxmidhar/verilog-and-systemverilog/1x8-demux-sv](https://github.com/Blaxmidhar/verilog-and-systemverilog/1x8-demux-sv)  
*Verified 1:8 demultiplexer functionality using class-based verification with randomized inputs and dynamic assertion checks for output lines.*
- 4:2 Encoder Testbench** [github.com/Blaxmidhar/verilog-and-systemverilog/priority-encoder-sv](https://github.com/Blaxmidhar/verilog-and-systemverilog/priority-encoder-sv)  
*Designed a functional verification environment for a 4:2 priority encoder to validate correct encoding of highest priority active input.*
- 4:16 Decoder Testbench** [github.com/Blaxmidhar/verilog-and-systemverilog/decoder-4x16-sv](https://github.com/Blaxmidhar/verilog-and-systemverilog/decoder-4x16-sv)  
*Constructed a structured testbench to verify one-hot output behavior of a 4:16 decoder based on binary control inputs.*

# UVM Concepts and Practical Implementation

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- Gained strong foundational knowledge of UVM testbench architecture including **test**, **env**, **agent**, **driver**, **monitor**, **sequencer**, **sequence**, and **scoreboard**.
- Learned the use of `uvm_config_db` for passing configuration data and virtual interfaces.
- Understood TLM (Transaction-Level Modeling) connections using analysis ports and exports for monitor-to-scoreboard communication.
- Studied sequence and sequence item classes using randomization, constraints, and factory registration.
- Gained hands-on experience in writing and registering components with macros like `\uvm_component_utils`.
- Learned how to control UVM phasing: build, connect, run, and report phases in testbench execution.
- Practiced using UVM reporting macros like `\uvm_info`, `\uvm_error`, etc.
- **Practical Work:** Based on this knowledge, I am implementing a UVM-based testbench to verify a simple adder. This includes defining custom transactions, stimulus generation through sequences, and response checking in a scoreboard.

## Publications

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1. Laxmidhar Barik, S. Samal, and A. Kumar, "Analysis and Optimisation of Sensitivity of AlN/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> based MOSHEMT pH Sensor," *Sensing and Imaging Journal*, (Communicated).
2. S. Samal, Laxmidhar Barik, A. Kumar, and G. P. Mishra, "GaN Heterostructure-Based MOSHEMT with an Embedded Cavity for Neutral Biomolecule Detection," in *2025 Devices for Integrated Circuit (DevIC)*, IEEE, Apr. 2025, pp. 380–384. doi: 10.1109/DevIC63749.2025.
3. Yogendra Kumar, Laxmidhar Barik, S.samal, and A. Kumar, "Sensitivity Analysis of pH Sensor using AlGaN/GaN MOS-HEMT Device for SiO<sub>2</sub>,Al<sub>2</sub>O<sub>3</sub>,HfO<sub>2</sub> ," in *2025 2nd international conference on Electronics and Computer Engineering*, EDAS Malaysia.(accepted)
4. Laxmidhar Barik, S.samal,Yogendra Kumar and A. Kumar, "Design of Highly sesnsitive AlN/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> based MOSHEMT as Bio-sensor ," in *2025 IEEE BIO-SENSORS 2025 USA*(Submitted)

## Technical Skills

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**Software & Hardware Languages:** C, C++, Verilog, VHDL, SystemVerilog, Unix, TCL.

**Design and Simulation Tools:** Intel Quartus Prime, Cadence Virtuoso, Xilinx Vivado, Silvaco TCAD, Xilinx ISE Design Suite, MATLAB, OriginPro, LTspice, HSPICE.

**Open source Tools:** EDA Playground,yosys,greynwolf,qflow,OpenSTA,Opentimer,Magic Layout editor,Ngspice,LTspice

## Experience

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- **Teaching Assistant – HDV (Hardware Design using Verilog)** Aug 2024 – Dec 2024  
Assisted Dr. Ashish Kumar in HDV (Hardware Design using Verilog). Conducted lab sessions on basic Verilog coding concepts including Half Adder, Full Adder, Encoders, Decoders, Flip-Flops, and FSM design. Supported students in simulations and debugging using tools like Xilinx ISE and Vivado.
- **Teaching Assistant – Computer Programming in C++** Jan 2025 – may 2025  
Assisted Dr. Prateek Dholakia in teaching B.Tech (1st semester) students the fundamentals of C++ programming. Covered topics such as data types, loops, functions, arrays, pointers, and object-oriented programming. Guided students through code debugging and hands-on lab sessions.

## Personal Details

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**Father's Name:** Priyanatha Barik  
**Address:** Nandanvihar Patia Bhubaneswar  
**Date of Birth:** 4<sup>th</sup> March 2000  
**Marital Status:** Unmarried  
**Gender:** Male  
**Nationality:** Indian  
**Languages Known:** English, Hindi, Odia